Upgrading Note
82C200 -> SJA1000

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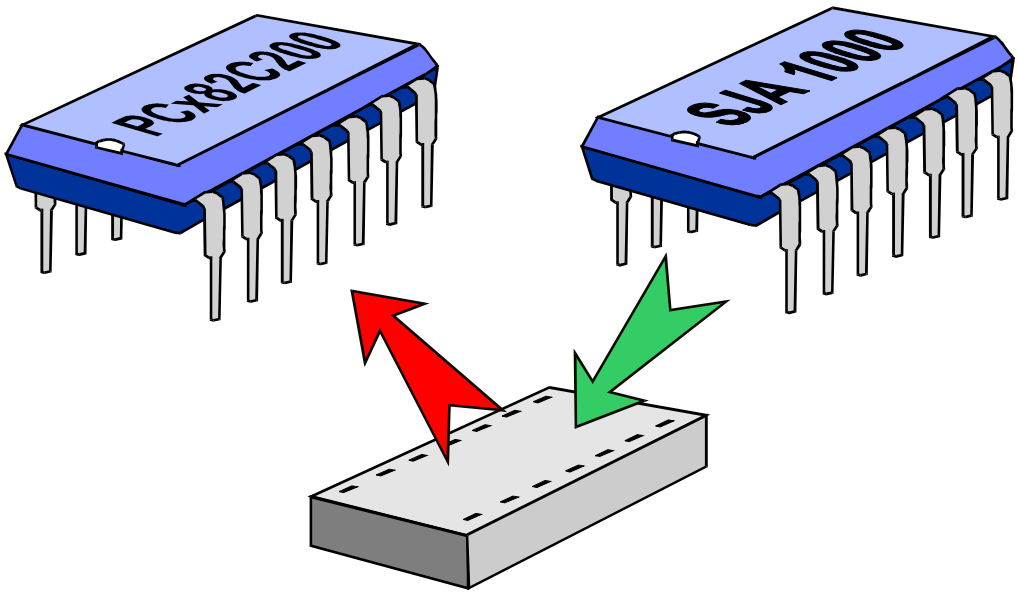

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1. General

The SJA1000 is the successor product for the PCx82C200 Stand-alone CAN Controller. It is software as well as hardware compatible to the 82C200 design. As the SJA1000 is a completely new design with a lot of new features (e.g. full CAN2.0B support), the following notes give a short overview, what hard- and software designers should consider if they migrate from the 82C200 to the SJA1000 for an existing design.

2. Hardware Compatibility

2.1 Package

Both package types are still available :

- DIL 28 (SOT117)
- SO28 (SOT136A)

2.2 Reset

The low active hardware reset input is now implemented with a defined hysteresis in order to increase the immunity at this pin.

2.3 Oscillator

The on chip oscillator allows frequencies from 6 up to 24 MHz. Due to the static design also frequencies lower than 6MHz are possible, if an external clock generator is used. Note, that frequencies below 6MHz are not tested in IC production.

2.4 Read / Write Interface

The SJA1000 allows much faster read and write accesses to its internal registers compared to the 82C200. Especially the low active $\overline{RD}$ and $\overline{WR}$ strobes may now be shortened from 170ns to approximately 60ns. The data hold times after a read access to the SJA1000 register are reduced from 55ns to 15ns max.

Note, that these timing informations are preliminary until the device is characterized. For more details please refer to the Data Sheet.

3. Software Compatibility

To keep software compatibility with the 82C200, the default mode of operation after hardware reset is the 82C200 compatibility mode (BasicCAN Mode).
In the BasicCAN Mode the SJA1000 emulates all known registers as defined for the 82C200 stand-alone CAN-controller. The following characteristics are different from the 82C200 design with respect to software compatibility.

3.1 Synchronization Mode

Because of the update to CAN 2.0B, the SYNC bit in the Control Register (CR.6 in the 82C200) has no functionality any more. Synchronization is possible only by a recessive-to-dominant transition on the CAN Bus. To keep software compatibility, writing and reading this bit is still viable.

3.2 Clock Divider Register

Most of the previously reserved bits of the Clock Divider Register are now used to activate certain new features of the SJA1000.
82C200 software, which writes no values greater than “07” to this register will still run on the SJA1000 without activating any of the new features and keep the SJA1000 in compatibility mode.

3.3 Receive Buffer

The dual message Receive FIFO concept of the 82C200 is replaced by a dynamic 64-byte Receive FIFO. Messages are stored with maximum density within the FIFO RAM what means, that there are no gaps between the messages.
The new FIFO allows to store at least 6 messages with 8 data bytes each. This has the positive effect, that the probability of “data overrun” conditions is reduced now. An overrun condition is signalled only, if the message to be stored within the FIFO is accepted and completed successfully (bit 6 of End Of Frame) but there was not enough free space to store it completely.

3.4 Transmission

Whenever the Reset Request bit is set automatically after bus-off or with CR.0, the Transmission Complete Status of the SJA1000 will keep unchanged.

Note that the 82C200 signals “complete” in this case.

3.5 CAN 2.0B

The SJA1000 is designed to fully support the Extended Frame message format as defined within the CAN 2.0B specification. Even in the 82C200 compatible mode the SJA1000 now tolerates Extended Frame messages on the bus in difference to the 82C200. That means that an acknowledgement is given if the message was correct. But due to the Message Buffer layout in the compatibility mode it is not possible to receive or transmit Extended Frame messages actively (CAN 2.0B “passive”).

3.6 Internal Command Processing

Within the 82C200 all commands were processed using the CAN bit clock, which was derived from the external clock frequency first divided by 2 and additionally divided by the user programmable Baud Rate Prescaler. The SJA1000 now just needs one internal clock period (external clock frequency divided by 2) to accept commands from the host CPU.

Overview of items to be considered when the SJA1000 is used for 82C200 designs

Item	82C200	SJA1000	improvements	restrictions
Hardware				
Temperature Range	-40 to +85 ^{o} C -40 to +125 ^{o} C	-40 to +125 ^{o} C	-	--
Reset Input ($\overline{RST}$)	without hysteresis	defined hysteresis (see data sheet)	increased noise immunity	-
Oscillator	3 to 16 MHz	6 to 24 MHz	better CAN performance (bit timing) possible	frequencies lower than 6 MHz only with external source
$\overline{RD}$ / $\overline{WR}$ pulse width [1)]	170 ns min.	60 ns min.	more flexible CPU interfacing	-
data float after RD high [1)]	55 ns max.	15 ns max.	more flexible CPU interfacing	-
Software				
SYNC Bit (Command Reg. CR.6)	CAN Bus synchronization on both edges	CAN Bus synchronization on recessive to dominant edge only	CAN2.0B compatible, CR.6 Flip Flop still exists but without effect	-
Clock Divider Register	bits 0 to 2 implemented only	all bits implemented except CDR.4	new modes selectable (“1”-active)	if the register is accessed, values greater than 7 not allowed
Receive FIFO	2 messages deep	64-bytes deep	much lower data overrun probability	-
Transmission	Reset Request sets Trans. Complete St. (TCS) = “complete”	Setting Reset Req. does not change the status of TCS.	TCS always reflects the status of the last transmission	waiting for TCS = “complete” upon setting Reset Request low is not allowed
CAN2.0B	not supported	supported	extended oscillator tolerance and CAN2.0B passive	-
Internal Command Processing [2)]	command needs at least (2 * BRP) / f_{OSC}	command needs at least 2 / f_{OSC}	faster reaction on commands	-

1) Note, that AC characteristics of the SJA1000 are subject to change slightly after characterisation of the device.

2) BRP : Baud Rate Prescaler; f_{OSC} : external oscillator frequency

4. Summary

The SJA1000 is a plug and play replacement of the 82C200. There are only three cases where the SJA1000 does not work in an 82C200 design:

- external crystal < 6 MHz
- Clock Divider Register has been written with a value greater than 7
- whenever the Transmission Complete Status is interpreted upon Reset Request.